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Performance Analysis of 3SSC and Multi VMC Based High Voltage Gain Dc-Dc Converter

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Abstract-The step up high voltage gain dc– dc converter with three state switching cell and five voltage multiplier cells provides continuous input current with reduced ripples and high voltage. The voltage increases by cascading several voltage multiplier cells constituted by diodes and capacitors that operate on the resonance principle. The voltage stress across the elements is reduced due to clamping performed by the output capacitor. Interleaving allows the operation of the multiplier stages with reduction of the current stress through the devices and the size of an input inductors and capacitors is also drastically reduced. It is suitable in cases where dc voltage step-up is demanded, such as electrical fork-lift, audio amplifiers and many other applications.

Key Terms—Boost converters, dc–dc converters, high voltage gain, voltage multiplier cells (VMCs).

I. INTRODUCTION

A DC-to-DC converter is a device that accepts a DC input voltage and produces a DC output voltage. Typically the output produced is at a different voltage level than the input. In addition, DC-to-DC converters are used to provide noise isolation, power bus regulation, etc. Boost converter is used when a higher output voltage than input is required.

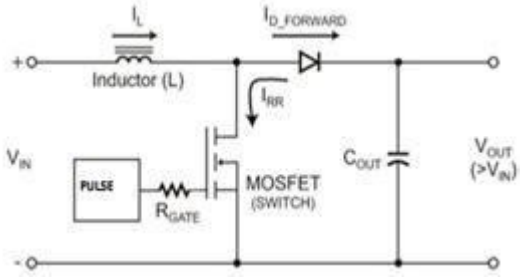

Fig.1. Boost Converter Circuit

While the transistor is ON $V_{IN} = V_{in}$, and the OFF state the inductor current flows through the diode giving $V_X = V_O$. For this analysis it is assumed that the inductor current always remainsflowing (Continuous conduction).The average voltage across the inductor must be zero for the average current to remain in steady state

$$V_{in}t_{on} + (V_{in}-V_O)\,t_{off}=0 \qquad (1)$$

this can be rearranged as

$$V_0/V_{in}=T/t_{off}=1/(1-D) \qquad (2)$$

And for a loss less circuit the power balance ensures

$$I_O/I_{in}= (1-D) \qquad (3)$$

Since the duty ratio "D" is between 0 and 1 the output voltage must always be higher than the input voltage in magnitude. The negative sign indicates a reversal of sense of the output voltage.

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II. DC-DC CONVERTER WITH VMC

The proposed dc-dc converter has 3ssc and 5 VMC cascaded to produce the high voltage gain. The topology used in the proposed method is that the two boost converters are coupled. So that the current is equally shared between two switches and the voltage doubler characteristics is also achieved. And also interleaving effectively reduces the input output current ripples. Hence the size of the energy storage inductor is reduced.

III. PROPOSED TOPOLOGIES

The main circuit diagram of proposed dc-dc converter with 3 state switching cells and five voltage multiplier cells is shows in fig.2.

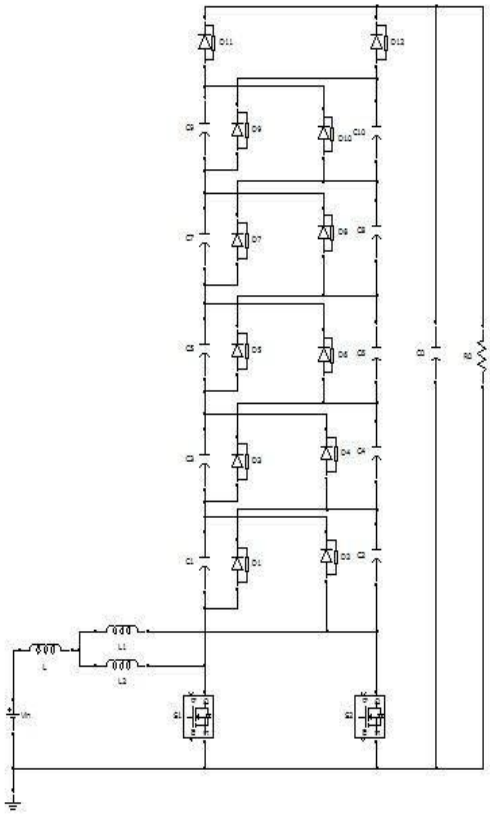

Fig.2.Circuit of Proposed Converter

In this circuit diagram the switches S1 and S2 are MOSFETs. These Metal oxide semiconductor field effect transistors with reduced on resistance can be used to minimize conduction loss. This proposed topology for voltage step-up applications based on the use of multiplier cells constituted by diodes and capacitors. The converter is able to operate in overlapping mode (when a duty cycle D is higher than 0.5) and non-overlapping mode (duty cycle is lower than 0.5).

OPERATING PRINCIPLE

Mode 1

Switches S1 and S2 are turned ON, while all Diodes are reverse biased. Energy is stored in

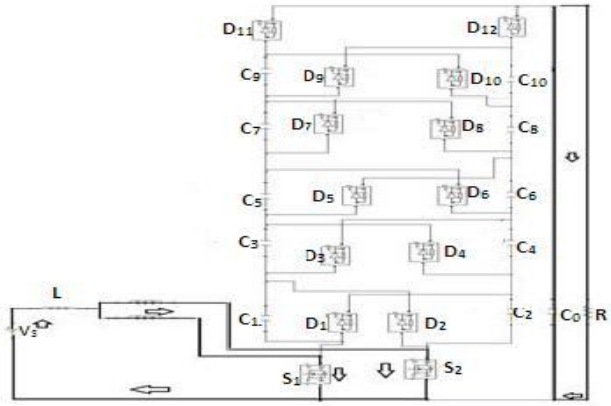

Fig.3.Mode1

Inductor L and there is no energy transfer to the load. The output capacitor provides energy to the load.

Mode 2

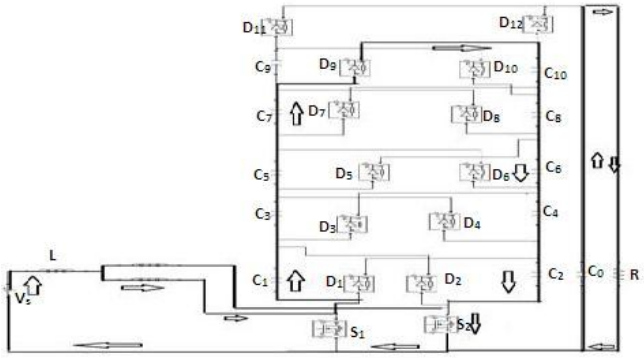

Fig.4.Mode 2

Switch S1 is turned OFF, while S2 is still turned ON and diodeD9 is forward biased. There is no energy transfer to the load as well. Inductor L stores energy,

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capacitors C1, C3, C5 and C7 are discharged, and capacitors C2, C4, C6, C8 and C10 are charged.

Mode 3

Switch S1 is turned OFF, while S2 is still turned ON and diode D7 is forward biased, while all

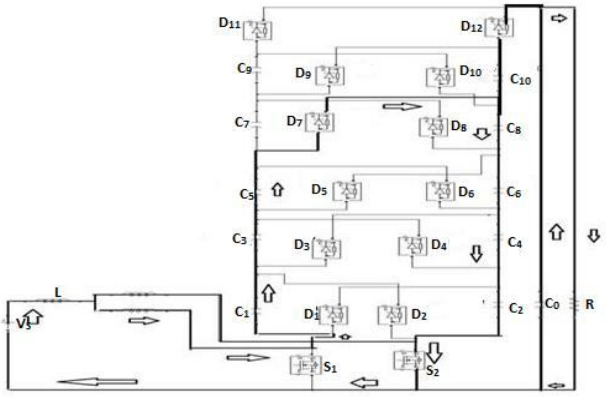

Fig.5.Mode3

the remaining ones are reverse biased. Energy is transferred to the output stage through *D12* .Inductor L stores energy, capacitors C1, C3 and C5 are discharged, and capacitors C2, C4, C6, C8 and C10 are charged.

Mode 4

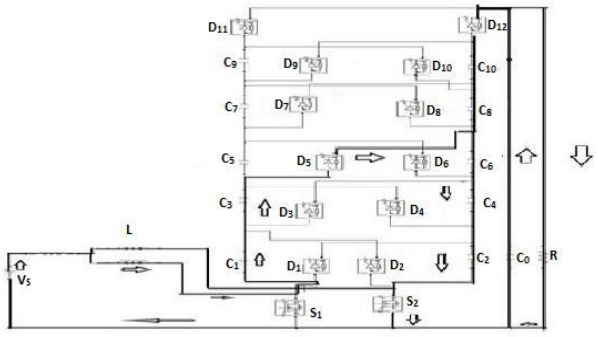

Fig.6.Mode 4

Switch S1 is turned OFF, while S2 is still turned ON and diodeD5 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through *D12*. Inductor L stores energy, capacitors C1 and C3 are discharged, and capacitors C2, C4, C6, C8, and C10 are charged.

Mode 5

Switch S1 is turned OFF, while S2 is still turned ON and diodeD3 is forward biased while all the remaining ones are reverse biased. Energy is transferred to the output stage through *D12*. Inductor L stores energy, capacitor C1 is discharged, and capacitors C_2, C4, and C6, C8, C10 are charged

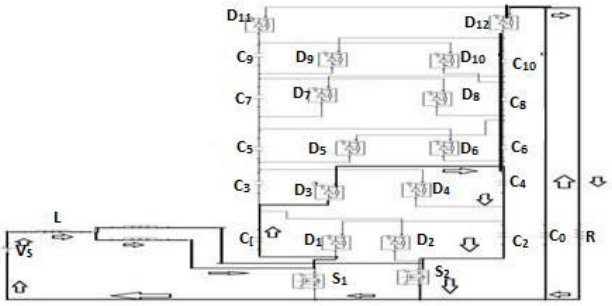

Fig.7.Mode 5

Mode 6

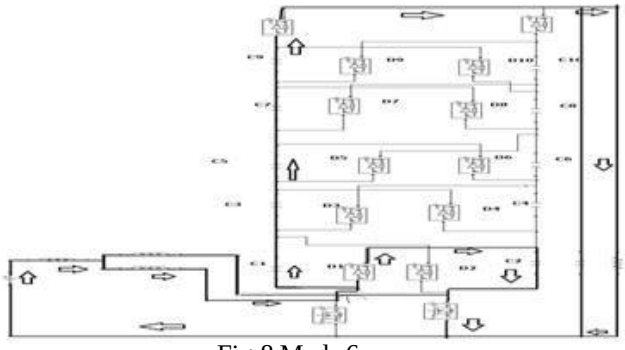

Fig.8.Mode 6

Switch S2 remains turned ON, diode D3 is reverse biased, and diode D1 is forward biased while all the remaining ones are reverse biased. Energy is transferred to the load through D11 . The inductor is discharged, and so are capacitors C1 , C3 , and C5

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, C7, C9 while C2 is charged.

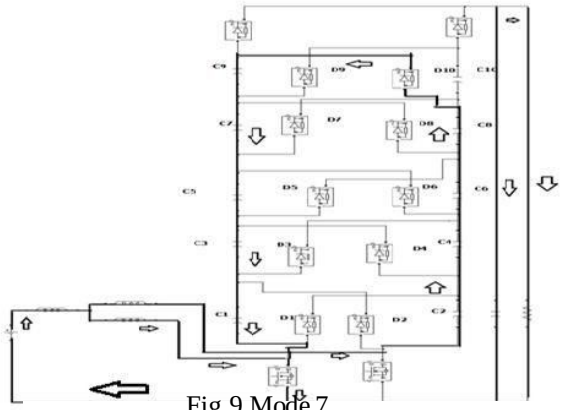

Fig.9.Mode 7

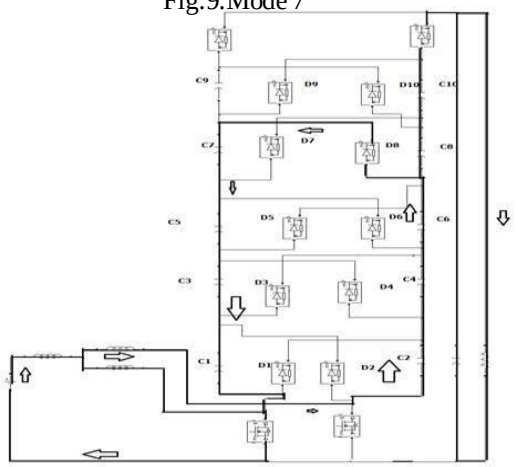

Fig.10.Mode 8

Switches S1 turned ON, DiodeD8 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through D12. The inductor stores energy and capacitors C1, C3, C5, and C7 are charged. Capacitors C2 are discharged, and so are C4, C6, C8, and C10.

Mode 9

Switches S1turned ON, Diode D6 is forward biased, while all the remaining ones are reverse

Mode 7

Switch S2 is turned OFF and switch S1 is still turned ON. Diode D10 is forward biased while all the remaining ones are reverse biased. The inductor is charged by the input source, although capacitors C2, C4, C6, and C8 are discharged and the capacitors C1, C3, C5, C7, and C9 are charged.

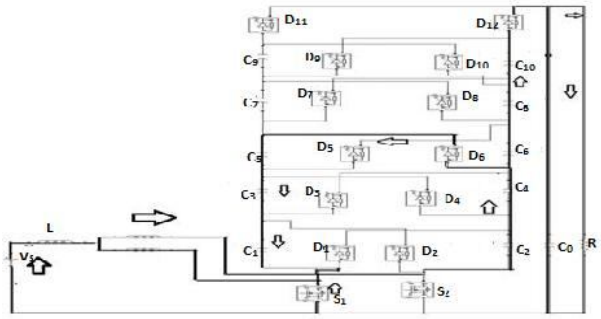

Fig.11.Mode 9

Biased. Energy is transferred to the output stage through D12. The inductor stores energy, and capacitors C1and C3, C5, are charged. Capacitors C2 are discharged, and so are C4 and C6, C8, C10.

Mode 10

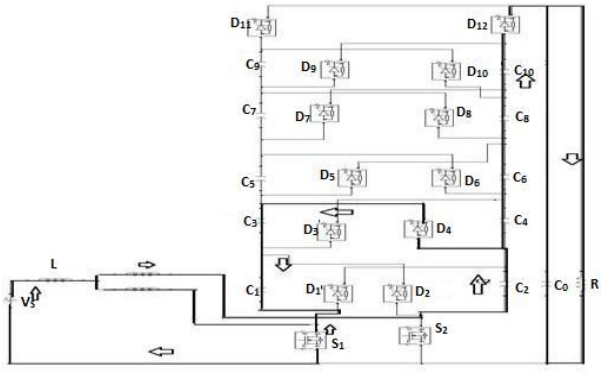

Fig.12.Mode 10

Switches S1turned ON, Diode D4 is forward biased, while all the remaini

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ng ones are reverse biased. Energy is transferred to the output stage through D12. The inductor stores energy and capacitors C1and C3 are charged. Capacitor C2 is discharged, and so are C4 and C6, C8, C10.

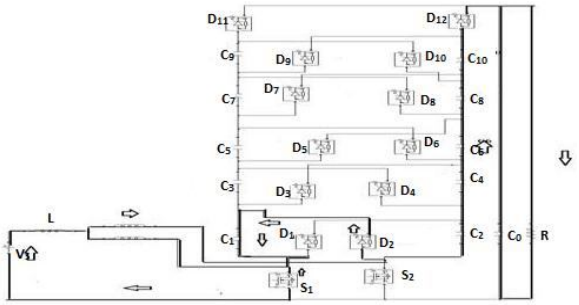

Fig.13.Mode 11

Energy is transferred to the output stage through D12. The inductor stores energy and capacitors C1 is charged. Capacitors C2 are discharged, and so are C4 and C6, C8, C10.

IV. DESIGN CALCULATION

Input voltage V_{in}=54V
Switching frequency
F_s=25KHz Multiplier cell =5
The maximum duty cycle is obtained using equation
$D= (V_0-V_i)*[(mc+1)/V_0]$
(5) D= 0.43
The ripple current is given by the equation
$\beta = (1-D)*[(2D-1) / (mc+1)]$ (6)
β=0.0716
The inductance value is calculated using equation
$L = V_0* \beta/ (2*f_s)$
(7) L=70µH
Where D = duty ratio
V = initial voltage
The capacitance value is calculated using equation
$C_n= (1-D) *V_{IN}*T_{on}$
For *n* = 1, 2, 3, *4, 5*

Mode 11

Switches S1turned ON, Diode D2 is forward biased, while all the remaining ones are reverse biased.

$C_1=C_2=4.4e^{-6}F$
$C_3=C_4=3.2 e^{-6}F$
$C_5=C_6=2.2 e^{-6}F$
$C_7=C_8=4.5 e^{-6}F$
$C_9=C_{10}=5 e^{-6}F$
The resistor value is calculated using the equation
$2f_c =$
R/2*3.14*L
R
=570ohms

V . SIMULATION RESULTS

The voltage increases by cascading several voltage multiplier cells constituted by diodes and capacitors. The voltage stress across the elements is reduced due to clamping performed by the output capacitor. The topology used in this method is that the two boost converters are coupled so that the current is equally shared between the switches and the voltage doubler characteristics is also achieved. The proposed structure with five multiplier cells has been designed and implemented with MATLAB-SIMULINK software. The input voltage of 54V is given and output voltage of 540V is obtained which is approximately ten times the input voltage

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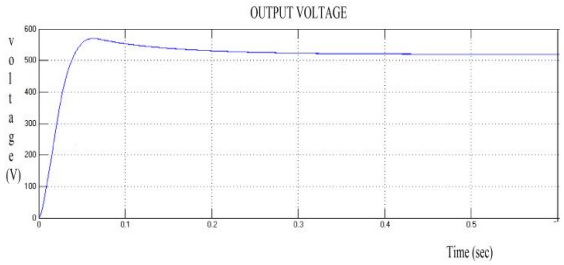

Fig.14.Output Voltage

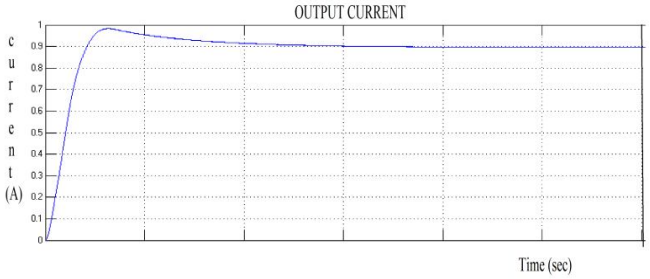

Fig.15.Output Current

VI. CONCLUSION

This project has proposed non isolated high voltage gain DC-DC converters. A novel high step up boost converter with voltage multiplier cell is presented. The voltage multiplier cell allows voltage to step up ten times its input while maintaining a moderate duty ratio. It is also expected that converters based on the 3SSC and 5VMC may be competitive solutions for high current and high voltage step up applications. Furthermore, only part of the energy from the input source flows through the active switches, while the remaining part is directly transferred to the load without being processed by these switches, i.e., this energy is delivered to the load through passive components, such as the diodes and the transformer windings The topology is adequate for several applications such as photovoltaic systems, fuel cell systems, UPS and Renewable energy.

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